

# 3-Dimensional Integrated Circuits

Aashana Pancholi

**Abstract**— With the advancement in technology as well as the manufacturing processes, the IC designs are becoming more and more complex, resulting in major design issues of placements and interconnections. Hence a new concept of 3 Dimensional IC is evolving which uses Through-Silicon Vias (TSV) to relax many bottlenecks related to IC designing. They also offer great performance along with high power. But with this new emerging technology, we need to think about its testing methodology from DFT point of view. Thus this paper is an overview of the entire manufacturing process of 3D IC with TSVs, the design challenges that one will face and the emerging testing approaches for 3D IC.

**Index Terms**— 3d IC with TSV, Manufacturing of 3d IC, Design Challenges in 3d IC, Testing approaches for 3d IC.

## 1 INTRODUCTION

As demands accelerate for increasing density, higher bandwidths, and lower power, many IC design teams are looking up – to 3D ICs with through-silicon vias (TSVs). 3D ICs promise “more than Moore” integration by packing a great deal of functionality into small form factors, while improving performance and reducing costs. Three-dimensional (3D) integration is promising technology to design integrated circuits (IC) with higher speed and smaller footprint than the ones designed by the traditional 2D IC design technologies. The idea behind 3D ICs/SiPs is to mount two or more dice on top of each other. An individual die is now so thin that theoretically it would be possible to mount 100 on top of each other to form a cube. For the monolithic manufacturing process using epitaxy, multiple device layers are grown on the same wafer in a serial manner. Once a layer of devices and their associated interconnect are completed, an isolation inter-level dielectric layer (for example, SiO<sub>2</sub>) can be deposited and polished to allow another layer of devices and interconnect to continue to grow vertically. To electrically connect devices across separate processed layers, 3D vias are etched through the isolation layer, and metal fillings are deposited. The same process is repeated to fabricate a 3D IC consisting of multiple layers of devices.

semblies may be categorized as 3D-ICs, but neither offers the performance, power, density, and form factor of true 3D-ICs using TSVs. What is new is the extension of the 3D package concept into the IC side.

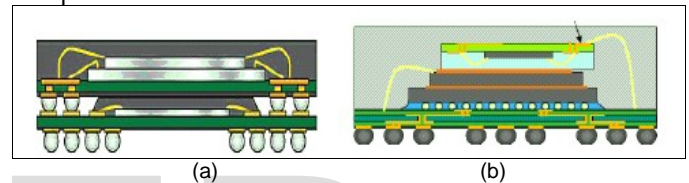


Fig. 2. A (a.) PoP and (b.) PiP packaged IC

3D packaging saves space by stacking separate chips in a single package. This packaging, known as System in Package (SiP) or Chip Stack MCM, does not integrate the chips into a single circuit. The chips in the package communicate using off-chip signaling, much as if they were mounted in separate packages on a normal circuit board. In contrast, a 3D IC is a single chip. All components on the layers communicate using on-chip signaling, whether vertically or horizontally. A 3D IC bears the same relation to a 3D package that a SoC bears to a circuit board.

## 2. 3D IC WITH TSV

A TSV is a vertical electrical connection passing through a silicon die. TSVs are copper vias with diameters that may range from 1 to 30 microns. A “true” 3D IC using TSVs involves two or more die connected together using TSVs. For example, consider a scenario in which one die containing TSVs is attached to the SiP substrate using conventional flip-chip technology. Meanwhile, a second die is attached to the first as illustrated in Figure 3. The configuration for 3D-IC shown here is referred to as a back-to-face (B2F) configuration, because the back of the first die is attached to the face of the second die. It is also possible to have back-to-back (B2B) and face-to-face (F2F) configurations, especially when more than two die are stacked in this manner.

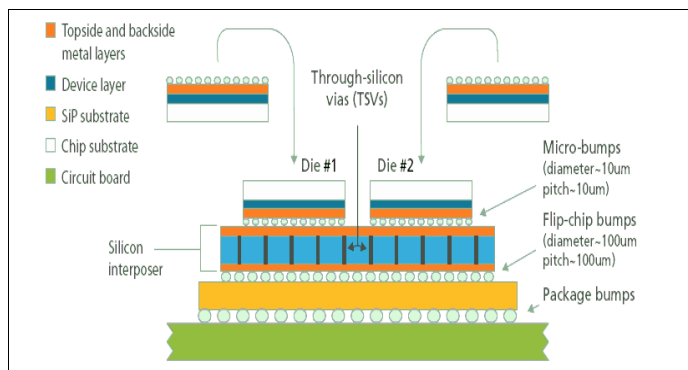


Fig. 1. A 3D IC

3D packaging has been around for years—stacks of die with wirebonds, package-in-package (PiP) design, and package-on-package (PoP) design, to name a few. PoP is a widespread configuration that combines a stack of memories on top of an application processor or digital baseband. Both PiP and PoP as-

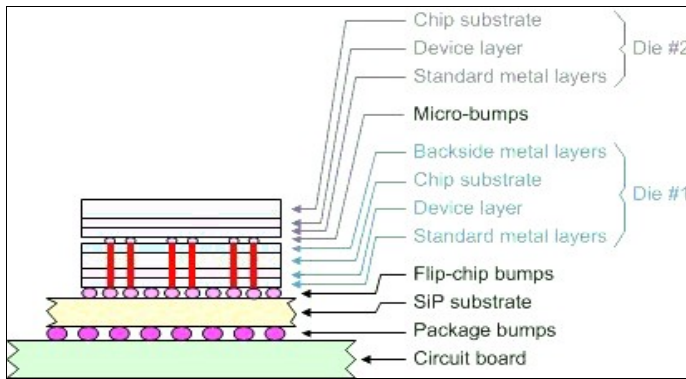


Fig. 3. Back-to-Face Configuration of a 3D IC with TSV

TSVs are a high performance technique used to create 3D packages and 3D integrated circuits, compared to alternatives such as package-on-package, because the density of the vias is substantially higher, and because the length of the connections is shorter. By using TSV technology, 3D ICs can pack a great deal of functionality into a small "footprint." The different devices in the stack may be heterogeneous, e.g. combining CMOS logic, DRAM and III-V materials into a single IC. In addition, critical electrical paths through the device can be drastically shortened, leading to faster operation.

Traditional single-die SoCs have some disadvantages. One is that all components are placed on the same die at the same process node, even though analog and RF design at advanced process nodes is extremely challenging. If a design team tries to implement analog circuitry at an advanced process node, it may take a great deal of time to develop and test the necessary IP blocks, as well as cope with process-related issues such as variability and leakage. Another challenge for single-die SoCs is mixed-signal integration and verification. Placing analog and digital circuitry in close proximity can cause many problems. Alternatively, sensitive analog or noisy digital components could be placed in a separate IC, but that makes it necessary to drive signals between individual packages, which consumes power and reduces performance.

In a 3D IC, a silicon interposer substrate (either passive or active) may be added to provide much finer die-to-die interconnections, thereby increasing performance and reducing power consumption. A silicon interposer also includes TSVs, which provide connections from the upper metal layers to additional backside metal layers.

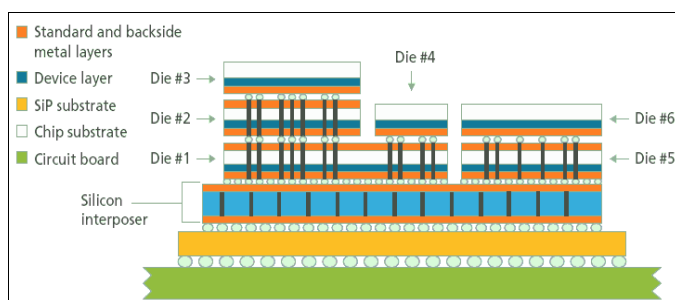


Fig. 4. A complex 3D IC with TSV and Silicon Interposer

## 2.1 Manufacturing of 3d IC

There are two main techniques of manufacturing a 3D IC. In terms of the process and the level of assembly that 3D ICs require, : Monolithic and Die-Stacking .

For the monolithic manufacturing process using epitaxy, multiple device layers are grown on the same wafer in a serial manner. Once a layer of devices and their associated interconnect are completed, an isolation inter-level dielectric layer (for example, SiO<sub>2</sub>) can be deposited and polished to allow another layer of devices and interconnect to continue to grow vertically. To electrically connect devices across separate processed layers, 3D vias are etched through the isolation layer, and metal fillings are deposited. The same process is repeated to fabricate a 3D IC consisting of multiple layers of devices. There is only one substrate, hence no need for aligning, thinning or bonding.

Another 3D integration technique is to stack individual 2D die layers vertically. In contrast to monolithic 3D manufacturing, which may require many changes in current process facilities, fabricating 3D ICs using die stacking technology can minimize the impact of altering existing manufacturing technology and equipment. With 3D die stacking, the candidate dies to be integrated onto the same package can be designed and manufactured separately, just as they are with a regular, existing 2D planar process with additional manufacturing processes of substrate thinning and through-silicon via (TSV) filling, if needed. Then they are bonded together by precise alignment of inter-die vias and the application of thermocompression. In general, die stacking presents three integration alternatives: wafer to wafer, die on wafer, and die on die, each with their respective pros and cons from a cost or yield perspective.

## 2.2 Design Challenges for 3d IC

While 3D-ICs with TSVs do not require a revolutionary new 3D design system, they do require some new capabilities that need to be added to existing tool sets for digital design, analog/custom design, and IC/package co-design. 3D-ICs require additional components to enable the 3D interconnections:

1. Redistribution layers (RDLs) are typically formed on the back side of the die. Bumps can thus be placed on both the front side and the back side.
2. TSVs can be drilled between the first metal layer and the back-side RDL. TSVs may have diameters from 1 to 5 microns.
3. "Micro-bumps" (much smaller flip-chip bumps) have to be aligned to create a data path from one die to another.

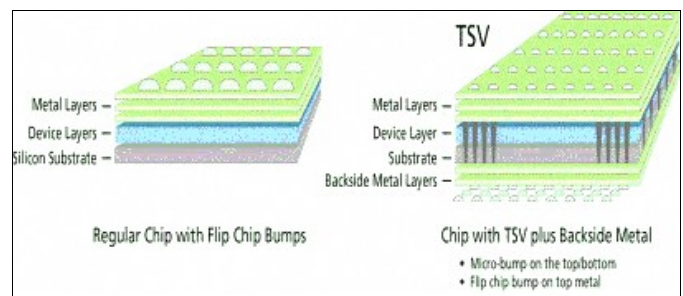


Fig. 5. Regular chip v/s. Chip with TSV

Since many 3D stacks combine digital and analog/RF circuitry, a strong analog/mixed-signal capability plus a robust IC/package co-design capability and PCB layout system are critical for providing a "complete" 3D-IC realization methodology. Without an integrated approach to 3D-IC design, optimizing system cost with the shortest possible turnaround time will be challenging.

In addition, new capabilities such as the following will be needed to meet 3D-IC design challenges:

- System-level exploration
- 3D floorplanning
- 3D implementation (placement, optimization, routing)
- 3D extraction and analysis
- 3D design for test (DFT)

### 3. TESTING APPROACHES FOR 3D IC

In traditional IC manufacturing, wafers are probed and individual dies tested (a process referred to as wafer sort) before they are packaged. In 3D integration, we are confronted with new challenges before bonding wafers. The yield of 3D ICs can be increased if we can bond pretested dies, or if we can sort the wafers first and stack matched dies (based on the speed or power consumption level) on top of each other. While wire-bonded systems-in-package (SiPs) may have a few hundred interconnects, 3D-ICs may have thousands if not tens of thousands of interconnects. Even a single defective TSV can render an entire stack unusable. If individual TSVs have 99.9% yield, at least one defective TSV can be expected in a stack of 1,000 TSVs.

A sound test methodology for 3D-ICs is necessary for IC designers to have the confidence to design them and to enable per-bond, midbond, post-bond, and post-package (final) testing. Fortunately, solutions are starting to emerge. 3D-IC testing can leverage a large body of technology and experience with modular SoC testing by using DFT wrappers and extending them to 3D testing. In the SoC world, modular testing is made possible by DFT wrappers such as the IEEE 1149.1 boundary scan standard and the IEEE 1500 embedded core test standard. For 3D-IC testing, these wrappers need to be enhanced with 3D-specific extensions such as the following:

- Additional probe pads for pre-bond testing
- Test "turnarounds" that start and finish the test access points at the bottom side of each die
- Test "elevators" that propagate test data vertically through the stack.

Like conventional single-die IC test, 3D IC test must be considered at two levels – wafer test (for the silicon die), and package test (after die assembly into the package). The difference is that in the 3D IC fabrication, there are many more intermediate steps, such as die stacking and TSV bonding. This provides many more opportunities for wafer test before final assembly and packaging.

Wafer test is needed for cost optimization. If a die is bad, it

can be thrown away before it is placed in a package. If a package-level test fails, the entire package would have to be thrown away. Thus, wafer test is highly desirable, especially early in the product lifecycle while defects may still be relatively high. But wafer test for 3D ICs is challenging for three reasons. First, today's probe technology is unable to handle the finer pitch and dimensions of TSV tips, and is generally limited to handling several hundred probes, whereas the TSVs may have several thousand probes. Second, probe technology leaves scrub marks that can potentially cause problems with the downstream bonding step. Finally, wafer test requires the creation of a known-good die (KGD) stack. To stack known-good die, the wafer must be thinned by about 75 percent so the tips of the TSVs can be exposed. However, as the thinned wafer is contacted by a wafer probe, there's a danger of damaging the wafer.

3D ICs also introduce new intra-die defects. These may be introduced by new manufacturing steps such as wafer thinning, or by bonding the top of a TSV to another wafer. Thermal effects are another potential sources of defects, because excessive heat may be generated from the densely packed stack of dies. Thermo-mechanical stress is caused by different thermal coefficients of the various materials in the stack. Despite the differences in the manufacturing steps, the resulting faults (shorts, opens, delay defects) appear to be similar to what we see in conventional ICs.

Modeling defects through TSV-based interconnects is a new area. These defects may be introduced in the fabrication or the bonding of TSVs. Fortunately, defects introduced through TSVs can be mapped to existing fault models, such as opens, shorts, static, delay, and bridging faults. However, a methodology is needed to map TSV defects to known fault types.

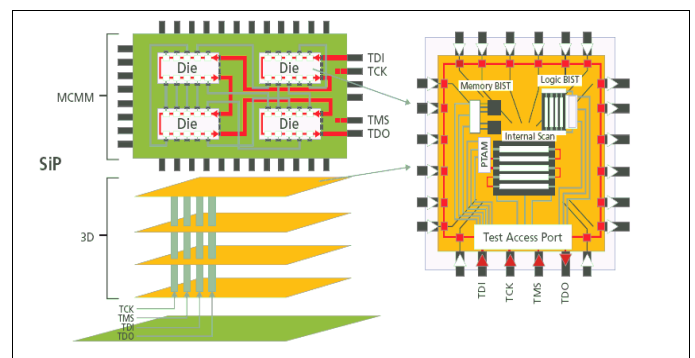


Fig. 6. Testing Approach to a 3D IC

#### 3.1 IEEE 1149.1 JTAG Test Approach for 3D IC

IEEE Std 1149.1 standardizes a test wrapper for chips on a Printed Circuit Board (PCB). It only has a serial mechanism, and lacks a higher bandwidth parallel test access mechanism. It has a two-bit (or optional three-bit) control port, consisting of the signals TCK, TMS, and optionally TRSTN. Internally, the additional control signals are generated by stepping through a 16-state finite state machine named TAP Controller.



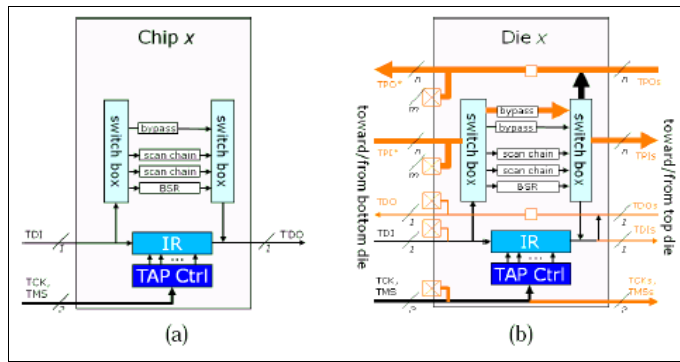


Fig. 7. IEEE 1149.1 JTAG Wrapper for (a.) Conventional and (b.) 3D IC

The 3D enhancements are highlighted in orange and comprise the following four items:

1. In order to support efficient high-volume testing of the die's circuitry, a parallel, scalable test port of user-defined width  $n$  is provisioned. We refer to the inputs and outputs of this port as resp. TPI and TPO.
2. Test Turns in every die, that feed test data back to the pins in the bottom die
3. There exist many alternative uses of IEEE 1149.1 beyond board-level interconnect testing for purposes like silicon and software debug, emulation, in-circuit programming, etc.

### 3.2 Scan Chain Design for 3D IC

In VLSI circuit design, scan chains are introduced to improve the testability of integrated circuits. After logic synthesis, all flipflops in the circuits are replaced with scan flipflops. These scan flip-flops are connected sequentially to form a scan chain (or multiple scan chains) in a single chip. Each scan flip-flop in the scan chain has two input sources: the output of the previous flip-flop in the scan chain and the output of the combinational circuits. During normal operation, the response at the state outputs is captured in the flipflop. In testing mode, test vectors are shifted into the registers through the primary input pads and the test output values are shifted out through the primary output pads. The output values are compared with expected values to examine if the circuit is working correctly or not.

Although the scan chain technique offers testing convenience, there is an area overhead coming from both multiplexed data flipflop and the routing of the stitching wires. Long stitching wires connecting the output of each flip-flop to the input of the next flip-flop increase the area of the circuit, make routing difficult, and influence test performance as well. Since one of the main objectives in design for testability is to minimize the impact of test circuitry on chip performance and cost, it is essential to minimize the wire length of a scan chain. Scan chain ordering techniques are used commonly in chip design to reduce wire length and circuit area. As technology scales, interconnect becomes the dominant source of delay and power consumption. Reducing interconnect delay and power consumption has become a major concern in deep submicron designs. Three-dimensional (3D) ICs are proposed as a promising solution to mitigate interconnect problems. In 3D chips,

multiple active device layers are stacked together with direct vertical interconnects, the TSVs.

When moving from the 2D IC design to the 3D IC design domain, there are several possible methods to connect the scan chain:

**Approach 1 (VIA3D):** The simplest way is to perform 2D scan chain insertion and ordering for each layer separately, and then connect  $N$  ( $N$  is the number of layers) scan chains into one single scan chain by using  $N - 1$  through silicon vias (TSVs). Fig. 8 illustrates such an approach: Nodes 1, 2, and 3 are connected to form a scan chain in layer 1; Nodes 4, 5, and 6 are connected to form a scan chain in layer 2. A through-silicon-via (TSV, the solid line in the figure) is then used to connect these two chains to be a single chain.

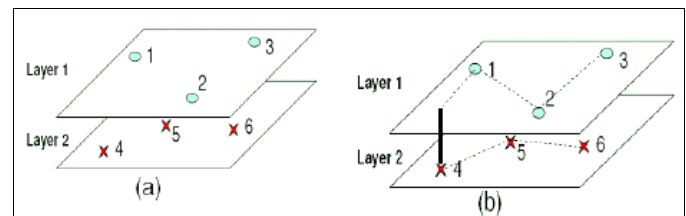


Fig. 8. (a) A conceptual example of 3D IC which has 3 scan cells to be connected. (b) VIA3D approach to connect each separate layer of scan chains via a single TSV

**Advantage:** Such an approach requires no change to the scan chain ordering algorithm: each layer is processed independently, with a 2D scan chain ordering algorithm. The resultant TSV number is minimized ( $N - 1$  TSVs for  $N$  layers).

**Disadvantage:** Because it is a locally optimized approach, it may result in the shortest scan chain for each layer, but the total scan chain length may not be globally optimized.

We call this method to be VIA3D scan chain ordering since the number of through silicon vias is minimized.

**Approach 2 (MAP3D):** Since the vertical distance between layers is small (in the range of 10  $\mu\text{m}$  to 100  $\mu\text{m}$ ), the second method is to transform a 3D scan chain ordering problem into a 2D ordering problem, by mapping the nodes from several layers into one single layer (i.e.,  $(x_i, y_i; L_i)$  is mapped to  $(x_i, y_i)$ ). A 2D scan chain ordering method is then applied to the design. Fig. 9 illustrates such an approach. After mapping the top layer nodes (Node 1, 2, and 3) onto the bottom layer, and performing 2D scan chain ordering, the scan chain order is 4-1-5-2-6-3. Based on such scan chain ordering, in 3D design, if two connected nodes are in different layers, a through silicon via (TSV) is used. In this example, there are 5 TSVs (the solid lines in the figure).

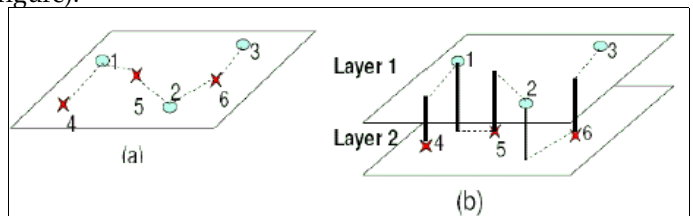


Fig. 9. Approach 2 (MAP3D): (a) All scan cells are mapped to 2D space. A 2D scan chain ordering method is then applied to the design. (b) The ordered connection is then done through TSVs.

**Advantage :** Such an approach requires no change to the scan chain ordering algorithm: after mapping all the nodes to a 2D plane, a 2D scan chain ordering algorithm is applied. It is a global optimization method.

**Disadvantage :** The vertical distance between layers is ignored. It may end up to using many TSVs going back and forth between layers.

We call this method to be MAP3D approach, because a 3D scan chain ordering problem is mapped to be a 2D scan chain ordering problem.

**Approach 3 (OPT3D):** The third approach is optimal (OPT) 3D ordering, from which we try to find the optimal solution for minimized wire length to form the scan chain. In this approach, the distance function includes horizontal cell-to-cell Manhattan distance between cells as well as vertical distance between two layers. In such case, we cannot apply a 2D scan chain ordering algorithm directly. The data structure (for example, the coordinates of a scan cell) may need to be modified. However, we take into account the 3D TSV effect (the length of TSVs and the number of TSVs) in the optimization, and can have full control of the optimization process: for example, we may apply constraints on how many TSVs can be used during scan chain ordering. Fig 10 illustrates such an approach.

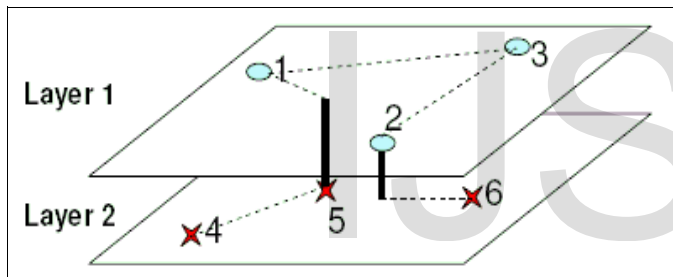


Fig. 10. A OPT3D approach of connecting and ordering the scan chains to optimize the minimum wire length.

**Advantage :** Such an approach is a true 3D scan chain ordering optimization: the length of TSVs and the number of TSVs are considered during optimization. Users have full control of the optimization process. It is a global optimization method.

**Disadvantage :** Modifications to 2D scan chain ordering algorithms are needed before they can be applied.

We call this method to be the OPT3D approach, because it is a true 3D scan chain ordering optimization approach.

During 3D design, one of these methods can be chosen according to the requirements, such as via number limitations and the easiness to implement. For example, one may want to reserve as many TSVs as possible for signal routing or for thermal conduction, and choose the VIA3D approach. On the other hand, if minimizing scan chain length is more important, and one does not want to make the effort to change the 2D scan chain algorithm, then the MAP3D approach can be adopted.

## 4 ADVANTAGES OF 3D IC

3-D integrated circuits were proposed invented to address the scaling challenge by stacking 2-D dies and connecting them in the 3<sup>rd</sup> dimension. This promises to speed up communication between layered chips, compared to planar layout. 3D ICs promise many significant benefits, including:

- Footprint

More functionality fits into a small space. This extends Moore's Law and enables a new generation of tiny but powerful devices.

- Cost

Partitioning a large chip into multiple smaller dies with 3D stacking can improve the yield and reduce the fabrication cost if individual dies are tested separately.

- Heterogeneous integration

Circuit layers can be built with different processes, or even on different types of wafers. This means that components can be optimized to a much greater degree than if they were built together on a single wafer. Moreover, components with incompatible manufacturing could be combined in a single 3D IC.

- Shorter interconnect

The average wire length is reduced. Common figures reported by researchers are on the order of 10-15%, but this reduction mostly applies to longer interconnect, which may affect circuit delay by a greater amount. Given that 3D wires have much higher capacitance than conventional in-die wires, circuit delay may or may not improve.

- Power

Keeping a signal on-chip can reduce its power consumption by 10-100 times. Shorter wires also reduce power consumption by producing less parasitic capacitance. Reducing the power budget leads to less heat generation, extended battery life, and lower cost of operation.

- Design

The vertical dimension adds a higher order of connectivity and offers new design possibilities.

- Circuit security

The stacked structure complicates attempts to reverse engineer the circuitry. Sensitive circuits may also be divided among the layers in such a way as to obscure the function of each layer.

- Bandwidth

3D integration allows large numbers of vertical vias between the layers. This allows construction of wide bandwidth buses between functional blocks in different layers. A typical example would be a processor+memory 3D stack, with the cache memory stacked on top of the processor. This arrangement allows a bus much wider than the typical 128 or 256 bits between the cache and processor. Wide buses in turn alleviate the memory wall problem.

## 5 DISADVANTAGES OF 3D IC

### · Yield

Each extra manufacturing step adds a risk for defects. In order for 3D ICs to be commercially viable, defects could be repaired or tolerated, or defect density can be improved.

### · Heat

Heat building up within the stack must be dissipated. This is an inevitable issue as electrical proximity correlates with thermal proximity. Specific thermal hotspots must be more carefully managed.

### · Design complexity

Taking full advantage of 3D integration requires sophisticated design techniques and new CAD tools.

### · TSV-introduced overhead

TSVs are large compared to gates and impact floorplans. At the 45 nm technology node, the area footprint of a  $10\mu\text{m} \times 10\mu\text{m}$  TSV is comparable to that of about 50 gates. Furthermore, manufacturability demands landing pads and keep-out zones which further increase TSV area footprint. Depending on the technology choices, TSVs block some subset of layout resources. Via-first TSVs are manufactured before metallization, thus occupy the device layer and result in placement obstacles. Via-last TSVs are manufactured after metallization and pass through the chip. Thus, they occupy both the device and metal layers, resulting in placement and routing obstacles. While the usage of TSVs is generally expected to reduce wirelength, this depends on the number of TSVs and their characteristics. Also, the granularity of inter-die partitioning impacts wirelength. It typically decreases for moderate (blocks with 20-100 modules) and coarse (block-level partitioning) granularities, but increases for fine (gate-level partitioning) granularities.

### · Testing

To achieve high overall yield and reduce costs, separate testing of independent dies is essential. However, tight integration between adjacent active layers in 3D ICs entails a significant amount of interconnect between different sections of the same circuit module that were partitioned to different dies. Aside from the massive overhead introduced by required TSVs, sections of such a module, e.g., a multiplier, cannot be independently tested by conventional techniques. This particularly applies to timing-critical paths laid out in 3D.

### · Lack of standards

There are few standards for TSV-based 3D-IC design, manufacturing, and packaging, although this issue is being addressed. In addition, there are many integration options being explored such as via-last, via-first, via-middle; interposers or direct bonding; etc.

### · Heterogeneous integration supply chain

In heterogeneously integrated systems, the delay of one part from one of the different parts suppliers delays the delivery of the whole product, and so delays the revenue for each of the 3D-IC part suppliers.

### · Lack of clearly defined ownership

It is unclear who should own the 3D-IC integration and packaging/assembly. It could be assembly houses like ASE or the product OEMs.

## 6 CHALLENGES TO IMPLEMENT 3D IC

Although 3-D integration shows promise, significant challenges associated with efficient circuit design and operation have hampered its adoption and further development. The most important issue in 3-D IC is heat dissipation. The thermal problem has already had an impact on the reliability and performance of high-performance 2-D ICs.

The problem is aggravated in 3-D ICs, principally for two reasons: the devices are more packed, which results in higher power density; and the insulating dielectric layers between the device layers have much lower thermal conductivities than silicon.

Furthermore, the third dimension brings both flexibility and difficulties to physical design algorithms. The existing 2-D metrics cannot be simply extended to generate similar metrics for 3-D designs. Take wirelength as an example: a "bounding-cube" might not have enough accuracy for wirelength estimation because of the existence of huge obstacles in z-direction.

Also, a 3-D IC physical design problem is usually of higher complexity, with a much enlarged solution space due to the multiple device layer structure. Efficient 3-D physical designs tools, including 3-D floorplanning, placement and routing tools, are essential to 3-D IC circuit design.

## 7 ACKNOWLEDGEMENT

I would like to indeed thank my mentors and guide Mr. Arif Makrani at eInfochips, Ahmedabad, my M.tech mentor and External Guide Mr. Nirav Nanavati from eInfochips, Ahmedabad and Mr. Bhavesh Soni my M.Tech internal guide from UVPCE, Ganpat University for inspiring and guiding me towards this research topic. Its a survey paper and the contents of this paper by me is an overall survey done on different papers already published and articles found on this subject. Hence I also want to acknowledge heartily each and every author who has done this research and helped me understand the concepts related to my survey paper.

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